REMARKS

In response to the Final Office Action mailed September 13, 2002, reconsideration is respectfully requested in view of the following remarks. To further the prosecution of this application, Applicants have addressed each of the issues raised in the Office Action, as discussed below.

Claims 1-52 are now pending in this application, of which claims 1, 5, 13, 17, 29, and 39 are independent claims. In this response, no claims have been amended. The application as now presented is believed to be in allowable condition.

A. Amendments to the Specification

Several typographical errors were found in the specification, and have been corrected herein. First, the paragraph beginning at line 28 of page 9 was rewritten to correct a mistyped reference to mixer 72, which should have been mixer 74. Second, the paragraph beginning at line 21 of page 20 was rewritten to correct the mistyped reference numerals 148, 149, and 150, which should have been S48, S49, and S50. The paragraph beginning at line 31 of page 13 was rewritten to correct a mistaken reference to Figure 3 which should have been a reference to Figure 6. The paragraph beginning at line 13 of page 14 has been amended to state that "in Fig. 7 and similarly labeled figures, the charges Q(C1)… Q(CN) represent the charge on capacitors C1… CN, respectively." This amendment is discussed in more detail below. The paragraph beginning at line 21 of page 25 has been amended to explicitly make note of the arrows in Fig. 24, and is also discussed below. Finally, the paragraph beginning at line 6 of page 31 has been amended to include the label SCF which was inadvertently omitted, and which was obviously intended to refer to the SC filter. The specification is now believed to be correct. These amendments will, if the application is not allowed, place the application in better form for appeal and reduce the issues on appeal.

B. Amendments to Drawings

Figures 4 and 5 have been amended to delete the spurious label 152. Fig. 6 has been amended to include (at the Examiner's suggestion) the waveform for P1 + P2,which is the logical OR of control signals P1 and P2. Figs. 17, 21-22, and 25 have been amended to delete the

unnecessary element label "NC". Figs. 28A-B have been amended to correct an erroneous label; specifically, the label "P3" has been deleted and replaced with the label "P2". Fig. 30 has been amended to delete the unnecessary labels "External Cap", "Voltage Output", and "Selectable Gain". These amendments are clearly supported by the specification, as discussed below, and introduce no new matter.

C. Rejections Under 35 U.S.C. §112, First Paragraph

Claims 1-52 were rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicants respectfully traverse these rejections.

The Office Action states at paragraph 2a that "it is not understood what number 152 and elements QDAC1 to QDACN in Fig. 4 really are and how they are interconnected with the [sic] and the charge sharing network since they are not described in the specification." Fig. 4, which merely serves as an illustrative block diagram, is described on page 11, line 28 to page 12, line 7. As discussed in the specification, the block diagram of Fig. 4 demonstrates the manner in which the multi-bit digital input is related to the analog output. Namely, the analog outputs QDAC1 through QDACN of the block diagram show signals which are indicative of a sum of values in the multi-bit signal. The purpose of this figure was merely to demonstrate generically some possible relationships between the digital inputs and the analog outputs, which are discussed later in more detail, along with the charge-sharing network. Therefore, it is believed that the specification does, in fact, describe all labeled elements of Fig. 4.

In paragraph 2b, the Office Actions states that "it is not understood what the number 152 in Fig. 5 really is since it is not described in the specification; it is not understood how switch S13 in Fig. 5 is controlled by P1 + P2 since the specification discloses that the P1 signal controls all switches S13-S16 (last line of page 13 and line 1 of page 14)." The Examiner apparently misreads the quoted passage. It does not say that switch S13 is controlled only by the P1 signal, but instead says that the P1 signal controls switch S13. This is correct. It is also true that the P2 signal (which is "OR'd" with the P1 signal) controls switch s13. The Office Action has failed to mention that switch S13 is also described as being controlled by phase 2 of the three-phase clock on lines 10-12 of page 14, where it is stated that the switch S13 is closed during the P2 phase of

the clock, along with switch S17, in order to provide an output to the output terminal 160. Thus, it is clear that one of the switches S13-S16, in this case S13, must be controlled by P1+P2 (i.e., the logical OR of P1 and P2), as is stated in the specification, in order to provide an output. Therefore, it is respectfully asserted that the operation and control of switch S13 is fully described in the specification and is consistent with the control signal shown in Fig. 5. While it is believed that Applicants have demonstrated ample support for the manner in which switch S13 is controlled, Fig. 6 has nonetheless been amended, as described above in the discussion of the amendments to the drawings, to explicitly show an additional signal which is derived from signals P1 and P2 and is the logical OR of those two signals.

In paragraph 2c, the Office Action states that "all equations on the right side of Figs. 7A-C, 8A-D and 12A-C, 14A-C, 19A-C, 33A-C and 24A-C are not understood since Vref is not shown in the drawings of the invention and Q(C1), Q(C2), Q(C3) and Q(C4) are not described in the specification." First, Applicants respectfully point out that it may be assumed that one skilled in any electrical art is familiar with the fact that the charge induced on a capacitor is equal to the capacitance of the capacitor times the voltage across the capacitor. This cannot be disputed. Consequently, using perfectly conventional notation, those skilled in the art will know that Q(C1) represents the charge (Q) on a capacitor C1, etc. Nonetheless, the specification has been amended in the paragraph beginning at page 14, line 13 to state that "the charges Q(C1)… Q(CN) represent the charge on capacitors C1… CN respectively." Secondly, Applicants point out that in the specification, reference is made to the fact the V1, V2, etc., which are stated in the specification to be the inputs to the switched capacitor DACs such as those shown in Figs. 5, 13, 16, 27, etc., may each be connected to unique input voltages, or may all be connected to a common voltage level which is called Vref. An example of this explanation can be found at page13, lines 16-26. As is known to those of ordinary skill in the art, a standard logic level, such as Vref, may be used to represent a logical 1 or 0 in a digital computing environment. In that way, the same voltage Vref may be present on two bit lines even though one bit line represents a value an order of magnitude higher than the other. For instance, a higher-valued bit line may be coupled to a capacitor with a capacitance which is scaled in relation to the value that the bit line represents. There is no need to show a voltage labeled Vref in the drawing as the specification makes it clear the Vref is not a reference element and thus it does not come under 37 C.F.R. 1.84. Consequently, the facts discussed above, which are certainly known to those skilled in the art,

coupled with the teachings of Applicant's specification, more than constitute support for the rejected.

The Office Action further states in its rejection that the switching ON/OFF operation of all the switches in each of Figs. 10, 11-A-D, 12A-C, 14A-C, 15, 16A-E, 17-18, 19A-C, 20-22, 25, 27, 30, 33A-C and 34A-C is not understood since no switching control signal associated with each of the switches is shown in the drawings and is described in the specification. Applicants strongly disagree. For each figure, the discussion of that figure in the specification gives detailed information about the timing and control of the various switches in the figure with respect to the phase signals P1-P4, when applicable. In some cases, for instance in Fig. 15, switches whose timing and control information is not discussed are explicitly stated to serve purposes other than switching. In the case of Fig. 15, these switches serve to balance parasitic effects which could harm performance. In other cases, the switch timing and control of some figures is not discussed because the timing of the same switches has already been explained in connection with other figures, as is the case with Figure 16. Respectively, for Figs. 10, 11, 12,14, 16-22, 25, 27, and 30, such discussions may be found at page 17, lines 11-26, page 18, lines 1-24; from page 18, line 25 to page 19, line 14; page 19, line 31 to page 20, line 16; from page 20, line 31, to page 25, line 7; page 26, lines 1-19; from page 27, line 14 to page 28, line 16; and from page 32, line 5 to page 31, line 14. Thus, Applicants respectfully assert that the switching operations of each of the figures in the specification are fully supported and that no additional drawing figure or text is needed. If the Examiner contends otherwise, he is respectfully requested to identify the specific switches whose controls, he believes, has not been adequately disclosed.

In paragraph 2e, the Office Action states that "it is not understood what element NC in Figs. 17, 21-22, 25 really is since it is not described in the specification." In response, the "NC" label has been removed, the control of the switches having been explained.

The Office Action states in paragraph 2f of the Office Action that "it is not understood what the four arrows on the right side of the scrambler 400 in Fig. 24 really are since they are not described in the specification." While Applicants respectfully assert that scramblers are well known to those skilled in the art of digital to analog conversion, and that figure 24 in conjunction with page 25, lines 21-32 is easily understood by any such person, the description of Fig. 24 beginning at page 25, line 21, has been amended to explicitly state that the scrambler "receives a

three bit digital input signal, bit_A, bit_B, bit_C, represented by the labeled arrows on the left, and outputs scrambled bits, represented by the arrows on the right."

The Office Action states that "it is not understood what the P3 in Figs. 28A-B really is since the specification discloses in line 5, page 30 that the conductor 454 is provided to supply the phase signal P2." Applicants have amended Figs. 28A-B to correct this typographical error. The description in the specification was correct as written, and Figs. 28A-B are now believed to agree with the specification.

In paragraph 2h, the Office Action states that "it is not understood what elements SCF, selectable gain, External CAP and Voltage output in Fig. 30 of the present invention really are since they are not described in the specification." The elements of Fig. 30 are described in the specification from page 31, line 6 to page 31, line 15. Fig. 30 is merely meant to provide an illustrative embodiment of the CT filter 92 shown in Fig. 2, and as such, is not described in great detail. However, Applicant has amended Fig. 30 to delete the "External CAP", "Voltage Output", and Selectable Gain" labels. Additionally, Applicant has amended the aforementioned paragraph to include the erroneously omitted label SCF, which refers to the SC filter.

Finally, the Office Action states in paragraph 2i that "it is not understood what elements $P1 + bit_1 \cdot P2$, $P1 + bit_2 \cdot P2$, $P1 + bit_3 P2$ and $P1 + bit_4 \cdot P2$ in Fig. 31 really [are] since they are not described in the specification." Applicants disagree, and respectfully point out that Figures 33A-33C and 34A-34C, along with the relevant portions of the specification (page 32, line 5 to page 33, line 16) explicitly show the relationship between the control signals input to the various switches of the squaring circuit in Figure 31 and the various clock phases P1-P3 and input bits bit_1-bit_4.

D. Rejections Under 35 U.S.C. §103

Paragraph 4 of the Office Action rejects claims 1-4 and 13-52 under 35 U.S.C. 103(a) as unpatentable over Fling et al., 4,591,832, in view of Mehta et al., 4,205,203, and Lee et al., 6,130,633. (It is noted that although claim 52 is listed as being rejected under 35 U.S.C. 103(a), this is believed to be a mistake since claim 52 depends from any of claims 5 or 12, which have been rejected under 35 U.S.C. 102 over Myers. Therefore, claim 52 is addressed later in conjunction with the rejection of claim 5.) Applicants respectfully traverse these rejections.

The Office Action does not address Applicants' previous response but repeats the previous rejection, verbatim. Applicant is entitled to a full and fair consideration of its arguments. Accordingly, Applicant can only repeat its arguments here and hope that the Examiner will now appreciate them.

1. <u>The Combination is Improper</u>

First, the Office Action provides no motivation from the prior art (whether the cited references or otherwise) to make the proposed combination. In order to establish a *prima facie* case of obviousness, there must be some suggestion or motivation in the prior art to make the proposed combination. The Examiner appears to be using the Applicants' own specification as the motivation for the proposed combination; that is hindsight and its use is improper. The Office Action has provided no motivation for the proposed combination in either Fling or Mehta or any other references; nor does one exist. Fling is directed to a system for processing the video information in a video signal (col. 1, lines 10-26). In order to enhance the image quality of certain digital video receivers, Fling attempts to double the number of horizontal lines displayed per frame while keeping the frame rate constant (col. 1, lines 27-35). This is because a television rasters the image onto the screen many times a second. Thus, video data is inherently serial; there is no need for a multi-bit DAC in the device of Fling, because Fling attempts to solve a problem which is inherently single bit. Not only would those skilled in the art have perceived no motivation to make the combination, but also it makes <u>no</u> <u>sense</u> to combine the multi-bit signal of Mehta with the device of Fling along with other references. Therefore, the rejection under 35 U.S.C. 103(a) over the combination of Fling and Mehta, where the use of a multi-bit signal would be inappropriate to Fling's intended use, is improper and should be withdrawn.

A break in the first link of a proposed combination destroys the whole chain of combination.

2. <u>Applicants' Claims Distinguish Over the Proposed Combination</u>

Even assuming *arguendo* that the proposed combination of Fling, Mehta, etc. did make sense and further assuming there was some hypothetical motivation, the proposed combination would still not meet and make obvious claims 1-4 and 13-51 of the present invention.

If one were to combine the teachings of Fling and Mehta, without reaching the tertiary references, one can posit that the resulting device would use the ping-pong DACs of Fling and

the multi-bit digital input of Mehta, as suggested on page 5 of the Office Action. Each bit of the multi-bit signal would enter a pair of pin-ponged DACs and would be converted to an analog signal at twice the rate as would be accomplished with only one of the DACs. However, such a device would neither anticipate nor make obvious any of claims 1-4 or 13-51, because, contrary to the assertion of the Office Action, Fling does not disclose a system having a DAC that receives a multi-bit digital signal and outputs *at least two* analog signals including a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal, the second analog signal also being indicative of said sum of values of the *same bits* in the multi-bit digital signal.

Firstly, Fling discloses only a DAC system having inside it **two DACs** (elements 16 and 18), **each of which output a *single* analog signal** (col. 2, lines 49-58). In contrast, claim 1 recites a system having **a DAC (i.e., a single DAC, not two) that receives a multi-bit digital signal and outputs at least *two* analog signals (i.e., one DAC, two output signals).** Secondly, those output signals include a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal and the second analog signal also being indicative of *the same* sum of values of said bits in the multi-bit digital signal. By contrast, each of Fling's ping-ponged DACs operate on *different* input bits and produces a *single* output. Neither of the DACs making up the DAC converter system of Fling, even when modified by Mehta to take in a multi-bit signal, outputs at least two analog signals, with or without the other two references, much less the claimed signals. Therefore, claim 1 is unobvious and patentably distinguishes over the combination of Fling and Mehta, and Applicants respectfully request that the rejection of claims 1-9 and 34-37 be withdrawn.

In addition, thirdly, nowhere in Fling or Mehta is it taught or suggested that the single analog value output by each of DACs 18 and 16 is indicative of a sum of bits. To the contrary, Fling shows, in Figs. 1 and 2, that the output of each DAC is a sample of *every other* value x_n, where x_n is the value of the single-bit signal x at time n. In other words, DAC 16 outputs a series of values x_{n-2}, x_n, x_{n+2}, etc., while DAC 18 outputs a series of values x_{n-3}, x_{n-1}, x_{n+1}, etc. In no way do *each* of DACs 18 and 16 of Fling output **two** analog signals, **each of which is indicative of a sum of bits**. Even the output 25 of the sum of the signals 20 and 22 is not indicative of a sum of bits; instead, it is indicative of an analog version of the time-varying single-bit signal 10.

Signals 20 and 22 are out-of-phase samples of the same, single-bit signal which combine to produce not two summed signals, but an analog version of the original signal.

Ignoring the fact that there is no demonstrated motivation to combine the ping-pong <u>video</u> converting DACs of Fling with the multi-bit <u>sound</u> signals of Mehta, if one of ordinary skill in the art were asked to combine the two by using one of Fling's one-bit ping-pong DAC systems for each bit of the multi-bit system, such a system would still not meet the claims of the present invention because 1) there would be no DAC that could output two analog signals, and 2) there would be no DAC which could output two analog signal indicative of a sum of values of bits, since each pin-pong DAC pair takes in a single-bit signal.

In contrast, claim 13, the second independent claim rejected over the combination of Fling and Mehta, recites a method comprising receiving a multi-bit digital signal and generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of ***said*** sum of values of said bits in the multi-bit digital signal. Claim 29 recites a similar method, and additionally recites providing at least two of the at least two analog signals to a signal conditioning stage, the at least two of the at least two analog signals including the first analog signal and the second analog signal.

As discussed above, nowhere in Fling or Mehta, or the other references, is it disclosed to generate at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of the same sum of values of the same bits in the multi-bit digital signal.

Claim 17 recites a system comprising means for receiving a multi-bit digital signal and means for generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal. Claim 39 also recites a similar system which also comprises means for generating at least two analog signals in response to a multi-bit digital signal, the at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital input signal and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal.

Thus, for the reasons cited above, claims 1-4 and 13-51 patentably distinguish over, and are not obvious in light of, the proposed combination of Fling, Mehta, and Lee. Consequently, the rejection of these claims under 35 U.S.C. 103(a) should be withdrawn.

E. Rejections Under 35 U.S.C. §102

Paragraph 6 of the Office Action rejects claims 5-12 under 35 U.S.C. §102(b) as anticipated by Myers, 5,798,724. (Applicants wish to point out that claim 52 has not been addressed in the rejection but depends from either of rejected claims 5 or 12; Applicants assume herein that the rejection is of claims 5-13 and 52. If, on the other hand, 52 was intended to be rejected as obvious over Myers in view of the combination of Fling/Mehta/Lee, the Office Action did not make that clear, and Applicant is not required to guess.) Applicants respectfully traverse this rejection.

1. Discussion of Myers

Myers is directed an interpolating digital to analog conversion system that reduces the spurious energy content of the output signal in an effort to reduce the order of monolithically integrated reconstruction filters (Abstract; col. 1, lines 26-40). Myers teaches having a first conversion stage 22 which converts the least significant n bits of an N-bit signal and a second conversion stage 30 for combining the remainder of the N bits with the output of the first conversion stage 22 to provide an amplitude value output in line 28 (col. 2, lines 58-64). An interpolation stage 30 interpolates the amplitude value output to provide an interpolated amplitude output at node 32 at an interpolation output rate which is a multiple of the input rate of the N-bit digital signal (col. 2, lines 65-67).

2. Applicants' Claims Distinguish Over Myers

Claim 5 recites a system comprising: a DAC that receives a sequence of digital input signals at an input data rate and outputs a sequence of analog signals to a signal conditioning stage at an output data rate, each of the analog signals being indicative of an associated one of the digital input signals, the magnitude of the output data rate being different than the magnitude

of the input data rate, wherein more than one of the analog signals is generated during a single digital to analog conversion cycle of the DAC.

Preliminarily, Applicants wish to point out that first conversion stage 22 of Myers, contrary to the Office Action's assertion, does not receive an N-bit data signal. Instead, as previously discussed, first conversion stage 22 *receives the n least significant bits* of an N-bit digital signal.

Myers fails to disclose or suggest the system of claim 5. In particular, nowhere does Myers disclose or suggest a system in which more than one of the analog signals is generated during a single digital to analog conversion cycle of the DAC.

The Office Action states in its rejection that Myers discloses in Fig. 1 a prior art system which comprises a finite impulse response filter 12 for generating a sequence of N-bit digital words at an interpolation rate, an N-bit DAC 14, and a reconstruct filter 16 which can be a switched capacitor filter. The Office Action further states that the prior art device of Fig. 1 can be implemented by the interpolating DAC 20 shown in Fig. 2. The Office Action states that the DAC 20 includes "a first conversion stage 22 receiving an N bit data signal at an input rate (see lines 56-60, column 2) and a second conversion stage 26 in combination with interpolation stage 30 for providing an output analog signal 32 at an interpolation rate which is a multiple of the input rate (see lines 64-67, column 2)."

However, nowhere does Myers suggest a system in which *more than one* of the analog signals is generated during a single digital to analog conversion cycle of the DAC. Indeed, the Office Action is completely silent regarding this aspect of the system recited in claim 5. Myers discloses that each of the conversion stages makes use of a switched capacitor array such as that shown in Fig. 4 for the digital to analog conversion (col. 3, lines 4-24 and 30-36). As discussed in Myers and shown in Figs. 3 and 4, each of the capacitor arrays 40 and 50 and the overall DAC system of Fig. 3 have a single output. In addition, the discussion of the operation of the capacitor array 40 shown in Fig. 4 makes it clear that only one output is provided by the capacitor array at output node 42, and that its output is provided at the sampling rate, as each of switches 44 are clocked at the sampling frequency (col. 3, lines 15-17). Thus, not only is it not disclosed or suggested to generate more than one of the analog signals during a single digital to analog conversion cycle of the DAC, but also it is *impossible* for the system of Myers to do so.

For at least the foregoing reasons, claim 5 patentably distinguishes over Myers. Accordingly, the withdrawal of the rejection of claim 5 under 35 U.S.C. §102(b) is respectfully requested.

Claims 6-12 and 52 depend from claim 5, and are believed to be allowable for at least the same reasons.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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x02/13/03

Marked-Up Specification

Please replace the paragraph beginning at line 28 of page 9 with the following rewritten paragraph:

--FIG. 1 is a block diagram of one embodiment of a portion of a handset 50 for a mobile communication system. The handset 50 includes an input portion having a transducer 54 that receives an input signal 56, e.g., a voice or other acoustical signal, representing information to be communicated via the mobile communication system. The transducer 54 converts the input signal 56 into an electrical signal, typically an analog signal, which is supplied to an analog-to-digital converter (ADC) 58, for example a voice band ADC. The ADC 58 periodically samples the electrical signal and generates a sequence of multi-bit digital signals, which are supplied to a digital baseband processor 60. The baseband processor 60 performs further signal processing, including for example, compression. The output of the baseband processor 60 is supplied to burst store stage 62, which feeds a GMSK modulator 64. The GMSK modulator 64 produces multi-bit digital signals, which is supplied via signal lines, represented by a signal line 66, to a digital to analog conversion system 68. The digital to analog conversion system 68 converts the sequence of multi-bit digital signals into an analog signal, which is supplied via signal line 70 to an output portion 72. The output portion 72 includes a mixer [72] <u>74</u> that receives the analog signal on signal line 70 and feeds a transmitter 76, which in turn transmits the signal. DAC can be used in any digital to analog conversion.--

Please replace the paragraph beginning on line 21 of page 20 with the rewritten paragraph shown below:

--FIG. 15 is a block diagram of another embodiment of the SC DAC 150, which is similar to the SC DAC 150 illustrated in FIGS. 9, 10A-10C, except that the SC DAC 150 of FIG. 15 further comprises a switch [148] <u>S48</u>, a switch [149] <u>S49</u>, and a switch [150] <u>S50</u>. A first terminal of the switch S48 is connected to the second terminal of the charge sharing switch S43. A first terminal of the switch S49 is connected to the second terminal of the charge sharing switch S45. A first terminal of the switch S50 is connected to the second terminal of the charge sharing switch S46. Each of the switches S48, S49, and S50 may, but need not serve one or more of the functions noted hereinbelow. In one embodiment, one purpose of the switches S48,

S49, S50 is to provide parasitic capacitance similar to that of output switch S47, so as to help cancel the effect of the parasitic capacitance of switch S47.--

Please replace the paragraph beginning at line 31 of page 13 with the following rewritten paragraph:

--The DAC 150 may receive a non-overlapping 3-phase clock, P1, P2, P3, shown in FIG. [3] <u>6</u>. The closed/open condition of the switches S3, S6, S9, and S12 is controlled by the P3 signal of the 3-phase clock. The P1 signal of the 3-phase clock controls the open/closed condition of the charge sharing switches S13, S14, S15, and S16. The P2 signal of the 3-phase clock controls the open/closed condition of the switch S17.--

Please replace the paragraph beginning at line 13 of page 14 with the following rewritten paragraph:

--FIGS. 7A-7C are block diagrams showing the operation of the SC DAC 150 of FIG. 5 for each of the 3 clock phases in the event that input terminals 172, 178, 184, and 190 are supplied with digital bit signals bit_1, bit_2, bit_3, bit_4, having logic states of 1, 0, 0, 0, respectively. Tables show the relationship between the clock phase, and the state (i.e., voltage and charge) of the capacitors in the one-bit DACs. <u>In Fig. 7 and similarly labeled figures, the charges Q(C1)… Q(CN) represent the charge on capacitors C1… CN, respectively</u>. Referring now to FIG. 7A, on phase P3 of the 3-phase clock, all of the charge sharing switches S13, S14, S15, and S16 and the output switch S17, are in the open condition. The capacitor C1 is charged to V_{ref} in response logic state 1 on terminal 172. Capacitors C2, C3 and C4 are all discharged to ground in response to the logic state 0 signals on terminals 178, 184, 190, respectively. Referring now to FIG. 7B, on phase P1 of the 3-phase clock, all of the charging switches S3, S6, S9 and S12 (FIG. 5) and the output switch S17 are in an open condition, and all of the charge sharing switches S13, S14, S15 and S16 are in a closed condition, whereby charge is redistributed and resulting in the total charge on all of the capacitors being divided among all of the capacitors. If the capacitors C1, C2, C3, C4 all have the same capacitance value C, then the charge is shared equally so that the voltage across each capacitor becomes $V_{ref}/4$. Referring now to FIG. 7C, on phase P2, charge

sharing switches S14, S15, and S16 are in the open condition, output switch S17 is in the closed condition, and capacitor C1 (FIG. 5) of one-bit DAC 162 delivers its charge to the output terminal 160. On the next occurrence of phase P3 (not shown), the multi-bit digital signal bit_1, bit_2, bit_3, and bit_4 may be updated and provided to the DAC 150 via input terminals 172, 178, 184, 190.--

Please replace the paragraph beginning at line 21 of page 25 with the following rewritten paragraph:

--FIG. 24 is a block diagram of one embodiment of a four bit scrambler 400 that receives a three bit digital input signal, bit_A, bit_B, bit_C, represented by the labeled arrows on the left, and outputs scrambled bits, represented by the arrows on the right. A scrambler is typically most effective when all of the scrambler inputs receive data . The extra input(s) of the scrambler may for example be "hardwired" to a logic state, i.e., a 1 or a 0. In this event that an input(s) of a scrambler is hardwired, it may be desirable to hardwire a corresponding number of DAC input(s), to a logic state opposite to that used for the extra input(s) of the scrambler.--

Please replace the paragraph beginning at line 6 of page 31 with the following rewritten paragraph:

FIG. 30 is a schematic diagram of one embodiment of the CT filter stage 92 of FIG. 2, which includes a two resistors R600, R601 that each receive an analog signal from the SC filter stage SCF, and form an RC filter with C600 and C601,to passively filter the images left by the switched capacitor filter. The images which appear at multiples of the SC filter sample rate. The stage may have selectable gain formed by an amplifier 600 and resistors R602-R607. The CT filter stage may further provide resistors R608, R609, which form a passive pole in combination with an off-chip capacitor C602. Although not required, the resistors in the output pole may be integrated to improve I/Q channel matching, reduce external component count and to reduce the effects of loading from the pin capacitance on the output stage amplifier.